IN THE CLAIMS

The current claims for this application are listed below:

1. (Currently amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated in response to changes in nominal system frequency while the PLL generating the clock signal; and

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory;

wherein a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable.

2. (Original) The clock circuit of claim 1, wherein the profile memory comprises static random access memory (SRAM).

3. (Original) The clock circuit of claim 1, wherein the profile state machine spread spectrum modulates the clock signal according to the plurality of entries.

4. (Original) The clock circuit of claim 1, wherein a position of the profile in the profile memory, read by the profile state machine in sequence to control the PLL, is adjustable.

5. (Original) The clock circuit of claim 4, wherein the profile memory further stores address information about the profile, the address information specifying the

number of entries of the profile and the position of the profile in the profile memory.

6. (Original) The clock circuit of claim 4, further comprising:

at least one register to store address information about the profile, the address information specifying the number of entries of the profile and the position of the profile in the profile memory.

7. (Original) The clock circuit of claim 1, wherein the profile memory is capable of simultaneously storing a plurality of profiles; and, the profile state machine is capable of being instructed to use one of the plurality of profiles to control the PLL.

8. (Original) The clock circuit of claim 7, wherein the profile memory stores address information for accessing the plurality of profiles at predetermined locations.

9. (Original) The clock circuit of claim 7, wherein the plurality of profiles comprise one profile for slewing the clock signal from a first nominal clock frequency to a second nominal clock frequency.

10. (Original) The clock circuit of claim 9, wherein the clock signal is slewed from the first nominal clock frequency to the second nominal clock frequency in managing at least one of:

a) power consumption; and

b) thermal status;

of the data processing system.

11. (Original) The clock circuit of claim 9, wherein the clock signal is slewed from the first nominal clock frequency to the second nominal clock frequency in balancing power consumption and computational load of the data processing system.

12. (Currently amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal through phase locking to a reference signal;

profile memory to store profile data comprising a plurality of entries, the profile memory capable of being updated while the PLL generating the clock signal; and

a profile state machine coupled to the profile memory and the PLL, the profile state machine to read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence from the profile memory;

wherein the profile memory is capable of simultaneously storing a plurality of profiles; and

wherein the profile state machine is capable of being dynamically instructed to use one of the plurality of profiles to control the PLL in response to changes in nominal clock frequency.

13. (Original) The clock circuit of claim 12, wherein the profile memory comprises static random access memory (SRAM).

14. (Original) The clock circuit of claim 12, wherein the profile state machine spread spectrum modulates the clock signal according to the plurality of entries

15. (Original) The clock circuit of claim 12, wherein the profile memory stores address information for accessing the plurality of profiles at predetermined locations

16. (Original) The clock circuit of claim 12, wherein the clock circuit is disposed on an integrated circuit (IC) chip.

17. (Original) The clock circuit of claim 12, wherein the clock circuit is capable of slewing the clock signal from a first nominal frequency to a second nominal frequency; and, the profile state machine is dynamically instructed to use one of the plurality of profiles for one of the first and second nominal frequencies.

18. (Original) The clock circuit of claim 17, wherein the clock signal is slewed to manage power and thermal status of the data process system.

19. (Original) The clock circuit of claim 12, wherein the plurality of profiles comprise a first profile for spread spectrum modulating the clock signal of a first nominal frequency; the plurality of profiles comprise a second profile for spread spectrum modulating the clock signal of a second nominal frequency; and the plurality of profiles comprise a third profile for slewing the clock signal between the first and second nominal frequencies.

20. (Currently amended) A machine implemented method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

in response to a change in nominal frequency, obtaining profile address information which specifies a location of a profile stored in profile memory, the profile corresponding to the new nominal frequency; and

reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL.

21. (Original) The method of claim 20, wherein the profile address information further specifies a size of the profile.

22. (Original) The method of claim 20, wherein the profile memory comprises static random access memory (SRAM).

23. (Original) The method of claim 20, wherein the clock signal is spread spectrum modulated according to the profile data.

24. (Original) The method of claim 23, wherein the address information is obtained from the profile memory.

25. (Original) The method of claim 20, further comprising:

updating a portion of the profile memory while the PLL generates the clock signal.

26. (Original) The method of claim 20; further comprising:

slewing the clock signal from a first nominal frequency to a second nominal frequency;

wherein the profile data of the profile is read in sequence to spread spectrum modulate the clock signal when the clock signal in the second nominal frequency.

27. (Original) The method of claim 26, wherein the clock signal is slewed from the first nominal clock frequency to the second nominal clock frequency to manage power consumption and computational performance.

28. (Currently amended) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal, the PLL capable of adjusting the clock signal frequency among a plurality of nominal frequencies;

means for obtaining profile address information which specifies a location of a profile stored in profile memory, the profile corresponding to a nominal frequency; and

means for reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL to adjust a nominal frequency of the clock signal.

29. (Original) The circuit of claim 28: wherein the profile address information further specifies a size of the profile.

30. (Original) The circuit of claim 28, wherein the clock signal is spread spectrum modulated according to the profile data.

31. (Original) The circuit of claim 28, wherein the address information is obtained from one of:

the profile memory; and

one or more registers.

32. (Original) The circuit of claim 28, further comprising:

means for updating a portion of the profile memory while the PLL generates the clock signal.

33. (Original) The circuit of claim 28, further comprising:

means for slewing the clock signal from a first nominal frequency to a second nominal frequency;

wherein the profile data of the profile is read in sequence to spread spectrum modulate the clock signal when the clock signal in the second nominal frequency.

34. (Original) The circuit of claim 33, wherein the clock signal is slewed from the first nominal clock frequency to the second nominal clock frequency to manage power consumption and computational performance.

35. (Currently amended) A machine implemented method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal in response to a change in clock signal from a first nominal frequency to a second nominal frequency,

wherein the profile memory is capable of being updated while the PLL generating the clock signal.

36. (Original) The method of claim 35, further comprising:

loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile, the second profile and a third profile;

spread spectrum modulating the clock signal at a first nominal frequency using the first profile;

slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile; and

spread spectrum modulating the clock signal at the second nominal frequency using the third profile.

37. (Original) The method of claim 35, further comprising:

loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile and the second profile.

38. (Original) The method of claim 35, further comprising:

replacing the first profile with a third profile in the profile memory.

39. (Original) The method of claim 38, wherein a size of the first profile is different from a size of the third profile.

40. (Original) The method of claim 38, further comprising:

switching from using the second profile to using the third profile stored in the profile memory for spread spectrum modulation of the clock signal.

41. (Original) The method of claim 35, further comprising:

slewing the clock frequency from a first nominal frequency to a second nominal frequency;

wherein the first profile is used for spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency.

42. (Original) The method of claim 41, wherein the second profile is used for spread spectrum modulation of the clock signal when the clock signal has the second nominal frequency.

43. (Original) The method of claim 41: wherein the second profile is used to slew the clock signal from the first nominal frequency to the second nominal frequency.

44. (Original) The method of claim 41, wherein the first nominal frequency is higher than the second nominal frequency; and, the clock frequency is slewed from the first nominal frequency to the second nominal frequency in response to a determination to reduce power consumption.

45. (Original) The method of claim 44, wherein the determination to reduce power consumption is in response to a measurement of a thermal sensor.

46. (Original) The method of claim 41, wherein the first nominal frequency is lower than the second nominal frequency; and, the clock frequency is slewed from the first nominal frequency to the second nominal frequency in response to a determination to increase computational performance.

47. (Currently amended) A machine readable medium containing executable computer program instructions which when executed by a data processing system

cause said system to perform a method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal in response to a change in clock signal from a first nominal frequency to a second nominal frequency,

wherein the profile memory is capable of being updated while the PLL generating the clock signal.

48. (Original) The medium of claim 47, wherein the method further comprises:

loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile, the second profile and a third profile;

spread spectrum modulating the clock signal at a first nominal frequency using the first profile;

slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile; and

spread spectrum modulating the clock signal at the second nominal frequency using the third profile.

49. (Original) The medium of claim 47, wherein the method further comprises:

loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile and the second profile.

50. (Original) The medium of claim 47, wherein the method further comprises:

replacing the first profile with a third profile in the profile memory.

51. (Original) The medium of claim 50, wherein a size of the first profile is different from a size of the third profile.

52. (Original) The medium of claim 50, wherein the method further comprises:

switching from using the second profile to using the third profile stored in the profile memory for spread spectrum modulation of the clock signal.

53. (Original) The medium of claim 47, wherein the method further comprises:

slewing the clock frequency from a first nominal frequency to a second nominal frequency;

wherein the first profile is used for spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency.

54. (Original) The medium of claim 53, wherein the second profile is used for spread spectrum modulation of the clock signal when the clock signal has the second nominal frequency.

55. (Original) The medium of claim 53, wherein the second profile is used to slew the clock signal from the first nominal frequency to the second nominal frequency.

56. (Original) The medium of claim 53, wherein the first nominal frequency is higher than the second nominal frequency; and, the clock frequency is slewed from the first nominal frequency to the second nominal frequency in response to a determination to reduce power consumption.

57. (Original) The medium of claim 56, wherein the determination to reduce power consumption is in response to a measurement of a thermal sensor.

58. (Original) The medium of claim 53, wherein the first nominal frequency is lower than the second nominal frequency; and, the clock frequency is slewed from the first nominal frequency to the second nominal frequency in response to a determination to increase computational performance.

59. (Currently amended) A data processing system, comprising:

a phase locked loop (PLL) to generate a clock signal;

means for dynamically switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal through the PLL in response to a change in clock signal from a first nominal frequency to a second nominal frequency.

60. (Original) The data processing system of claim 59, further comprising:

means for loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile: the second profile and a third profile;

means for spread spectrum modulating the clock signal at a first nominal frequency using the first profile;

means for slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile; and

means for spread spectrum modulating the clock signal at the second nominal frequency using the third profile.

61. (Original) The data processing system of claim 59, further comprising:

means for loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile and the second profile.

62. (Original) The data processing system of claim 59, further comprising:

means for replacing the first profile with a third profile in the profile memory.

63. (Original) The data processing system of claim 62, wherein a size of the first profile is different from a size of the third profile.

64. (Original) The data processing system of claim 62, further comprising:

means for switching from using the second profile to using the third profile stored in the profile memory for spread spectrum modulation of the clock signal.

65. (Original) The data processing system of claim 59, further comprising:

means for slewing the clock frequency from a first nominal frequency to a second nominal frequency;

wherein the first profile is used for spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency.

66. (Original) The data processing system of claim 65, wherein the second profile is used for spread spectrum modulation of the clock signal when the clock signal has the second nominal frequency.

67. (Original) The data processing system of claim 65, wherein the second profile is used to slew the clock signal from the first nominal frequency to the second nominal frequency.

68. (Original) The data processing system of claim 65, wherein the first nominal frequency is higher than the second nominal frequency; and, the clock frequency is slewed from the first nominal frequency to the second nominal frequency in response to a determination to reduce power consumption.

69. (Original) The data processing system of claim 68, wherein the determination to reduce power consumption is in response to a measurement of a thermal sensor.

70. (Original) The data processing system of claim 65, wherein the first nominal frequency is lower than the second nominal frequency; and, the clock frequency is slewed from the first nominal frequency to the second nominal frequency in response to a determination to increase computational performance.

71. (Original) A machine implemented method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

slewing the clock signal from a first nominal frequency to a second nominal frequency using first profile data stored in profile memory of a clock circuit, the first nominal frequency being substantially different from the second nominal frequency.

72. (Original) The method of claim 71, wherein the first profile data is used repeatedly to slew the clock signal from the first nominal frequency to the second nominal frequency.

73. (Original) The method of claim 72, wherein the clock signal is slewed from the first nominal frequency to the second nominal frequency in a substantially linear variation with respect to time.

74. (Original) The method of claim 72, wherein the profile memory further stores second profile data; and, the method further comprises:

spread spectrum modulating the clock signal using the second profile data after the clock signal is slewed to the second nominal frequency.

75. (Original) A clock circuit for a data processing system, the circuit comprising:

a phase locked loop (PLL) to generate a clock signal;

profile memory to store first profile data;

a profile state machine coupled to the profile memory and the PLL, the profile state machine controlling the PLL to slew the clock signal from a first nominal frequency to a second nominal frequency using the first profile data stored in the profile memory, the first nominal frequency being substantially different from the second nominal frequency.

76. (Original) The circuit of claim 75, wherein the first profile data is used repeatedly to slew the clock signal from the first nominal frequency to the second nominal frequency.

77. (Original) The circuit of claim 76, wherein the clock signal is slewed from the first nominal frequency to the second nominal frequency in a substantially linear variation with respect to time.

78. (Original) The circuit of claim 76, wherein the PLL is an n-phase PLL; and each entry of the first profile data selects one of n phased outputs of the PLL.

79. (Original) A machine readable medium containing executable computer program instructions which when executed by a data processing system cause said system to perform a method to control a frequency of a clock signal generated by a phase locked loop (PLL), the method comprising:

instructing a clock circuit to slew the clock signal from a first nominal frequency to a second nominal frequency using first profile data stored in profile memory of the clock circuit, the first nominal frequency being substantially different from the second nominal frequency.

80. (Original) The medium of claim 79, wherein the first profile data is used repeatedly to slew the clock signal from the first nominal frequency to the second nominal frequency.

81. (Original) The medium of claim 80, wherein the clock signal is slewed from the first nominal frequency to the second nominal frequency in a substantially linear variation with respect to time.

82. (Original) The medium of claim 80, wherein the profile memory further stores second profile data; and, the method further comprises:

instructing the clock circuit to spread spectrum modulate the clock signal using the second profile data after the clock signal is slewed to the second nominal frequency.

83. (Original) The medium of claim 79, wherein the clock signal is slewed in response to a determination to adjust one of:

power consumption;

thermal condition; and

computation performance.

84. (Original) A data processing system, comprising:

a clock circuit having profile memory storing first profile data;

means for instructing a clock circuit to slew the clock signal from a first nominal frequency to a second nominal frequency using the first profile data stored in the profile memory of the clock circuit, the first nominal frequency being substantially different from the second nominal frequency.

85. (Original) The data processing system of claim 84, wherein the first profile data is used repeatedly to slew the clock signal from the first nominal frequency to the second nominal frequency.

86. (Original) The data processing system of claim 85, wherein the clock signal is slewed from the first nominal frequency to the second nominal frequency in a substantially linear variation with respect to time.

87. (Original) The data processing system of claim 85, wherein the profile memory further stores second profile data; and, the data processing system further comprises:

means for instructing the clock circuit to spread spectrum modulate the clock signal using the second profile data after the clock signal is slewed to the second nominal frequency.

88. (Original) The data processing system of claim 84, wherein the clock signal is slewed in response to a determination to adjust one of:

power consumption;

thermal condition; and

computation performance.